Amendments to the Claims

This listing of claims replaces all prior versions and listings of claims in the application.

Listing of Claims:

1. (Currently Amended) A design method of a semiconductor integrated circuit:

wherein the semiconductor integrated circuit comprising a plurality of logic blocks comprises:

first logic circuits each including a first group of registers to which [[an]] external data is written in a first latching ~~firstly~~ step after the external data is input and a first control circuit for controlling the first group of ~~resisters;~~ registers; and

second logic circuits each including a second group of registers to which the external data is not written in ~~a second~~ the first latching step ~~firstly after the external data is input~~ and a second control circuit for controlling the second group of registers in accordance with a first output signal from the first logic ~~circuit,~~ circuits,

wherein the design method comprises the steps of:

first designing layout and timing verification of the first logic circuits and first control lines and first data lines between the plurality of logic blocks; and

second designing layout and timing verification of one of the second logic circuits.

2. (Currently Amended) The design method of the semiconductor integrated circuit according to claim 1,

wherein each of the second logic circuits comprises a plurality of logic sub-blocks comprising:

[[a]] third logic circuits each including a third group of registers to which [[a]] data input to each of the second logic ~~circuit~~ circuits is written in a ~~third~~ second latching ~~firstly~~ step after

the data [[being]] is input and a third control circuit for controlling the third group of registers; and

a fourth logic circuit including a fourth group of registers to which the data input to each of the second logic ~~circuit~~ circuits is not written in ~~a fourth~~ the second latching step ~~firstly after the data being input~~ and a fourth control circuit for controlling the fourth group of registers in accordance with a second output signal from the third logic ~~circuit,~~ circuits,

wherein the second designing layout and timing verification step comprises:

designing layout and timing verification of the third logic circuits and second control lines and second data lines between the plurality of logic sub-blocks; and

designing layout and timing verification of ~~one of~~ the fourth logic ~~circuits.~~ circuit.

3. (Currently Amended) A semiconductor integrated circuit comprising:

a plurality of logic blocks each comprising:

a first logic circuit including a first group of registers to which [[an]] external data is written in a first latching step ~~firstly~~ after the external data is input and a first control circuit for controlling the first group of ~~resisters;~~ registers; and

a second logic circuit including a second group of registers to which the external data is not written in ~~a second~~ the first latching step ~~firstly after the external data is input~~ and a second control circuit for controlling the second group of registers in accordance with a first output signal from the first logic circuit,

wherein the first logic circuit and the second logic circuit are disposed separately.

4. (Currently Amended) The semiconductor integrated circuit according to claim 3,

wherein ~~each of the logic blocks~~ the second logic circuit comprises a plurality of logic sub-blocks each comprising:

a third logic circuit including a third group of registers to which [[a]] data input to ~~each of~~ the second logic circuit is written in a ~~third~~ second latching step ~~firstly~~ after the data being input and a third control circuit for controlling the third group of registers; and

a fourth logic circuit including a fourth group of registers to which the data input to ~~each of~~ the second logic circuit is not written in ~~a fourth~~ the second latching step ~~firstly after the data being input~~ and a fourth control circuit for controlling the fourth group of registers in accordance with a second output signal from the third logic circuit, and

wherein the third logic circuit and the fourth logic circuit are disposed separately.

5. (Currently Amended) The semiconductor integrated circuit according to claim 3, wherein ~~the first group of registers is constituted by a register to which~~ the external data is directly input to the first group of registers.

6. (Original) The semiconductor integrated circuit according to claim 3,

wherein each of the logic blocks comprises a circuit for adjusting timing of a generated control signal and the control signal is not output from each of the logic blocks.

7. (Currently Amended) A design tool of a semiconductor integrated circuit:

wherein the semiconductor integrated circuit comprising a plurality of logic blocks comprises:

first logic circuits each including a first group of registers to which [[an]] external data is written in a first latching ~~firstly~~ step after the external data is input and a first control circuit for controlling the first group of ~~resisters;~~ registers; and

second logic circuits each including a second group of registers to which the external data is not written in ~~a second~~ the first latching step ~~firstly after the external data is input~~ and a second control circuit for controlling the second group of registers in accordance with a first output signal from the first logic ~~circuit;~~ circuits;

wherein the design tool executes:

a first design step for designing layout and timing verification of the first logic circuits and first control lines and first data lines between the plurality of logic blocks; and

a second design step for designing layout and timing verification of one of the second logic circuits.

8. (Currently Amended) The design tool of the semiconductor integrated circuit according to claim 7,

wherein each of the ~~logic blocks~~ second logic circuits comprises a plurality of logic sub-blocks each comprising:

a third logic circuit including a third group of registers to which a value can be externally written in a ~~first~~ second latching step after external data being input and a control circuit for controlling the third group of registers; and

a fourth logic circuit including a fourth group of registers to which a value cannot be externally written in ~~a first~~ the second latching step ~~after external data being input~~ and a control circuit for controlling the fourth group of registers in accordance with an output signal from the third logic circuit, and

wherein the second design step ~~executes:~~ comprises:

a third design step for performing layout and timing verification of a logic circuit that includes a signal line between the logic sub-blocks and the third logic circuit; and

a fourth design step for performing layout and timing verification of the fourth logic circuit in each of the logic sub-blocks independently.